

10th Chilplet/3D Test Workshop

Final Program

Grand Hyatt River Walk, San Antonio, Texas
Thursday, October 15- 16, 2026

16:00 - 16:10 **Opening Remarks – Yervant Zorian** (Synopsys Inc.), General Chair
Saman Adham, Program Chair

16:10 – 17:00 Keynote Address

Chair: Anshuma Chandra, Siemens EDA

Meg O’Brien, Director of Product Engineering at Lightmatter Inc.

17:00 - 18:30 Session 1: IEEE P3405 update

Chair: Vinay Kotha, Cisco Systems

17:00 - 17:30 **“A Novel Standard Approach of Test & Repair Architecture for Interconnects Between Chiplets in 3D/2.5D packages”**, Tapan Chakrabarty, Renesas Electronics America

17:30 – 18:00 **“Interconnect Test and Repair Language (ITRL) for Chiplets and 3D IC Packages”**
Anshuman Chandra, Siemens EDA.

18:00 – 18:30 **“Defects in Die-to-Die Interconnects, Cluster Effects & Impact on Repairability”**,
Moiz Khan, CISCO Systems Inc.

18:30 – 20:00 Workshops Reception

Friday, October 16

8:30 - 10:00 Session 2: Optical/Photonic devices Testing in Chiplet/3D IC Chair: Lawrence van Der Vegt, MPI Corporation

8:30 – 9:00 “Scaling Optical Test Strategies for Co-Packaged Optics (CPO)”

Ines Brunn, Global Business Development & Product, Strategy Leader at VIAVI Solutions

9:00 – 9:30 “Laser-Based Trimming and Cleaning Solutions: Enabling Scalable CPO Manufacturing”

Louis-Rafaël Robichaud, CEO and Co-Founder at Femtum

9:30 – 10:00 “Testing of Electro-Optic Co-Packaged and Double-Sided chip architectures”

Lawrence van der Vegt, Head of Photonics AST at MPI Corporation

10:00 - 10:15 Coffee Break

10:15 - 11:15 Panel: Security in Chiplet/3D Test Moderator: Moiz Khan, Cisco Systems

Panelists:

Prof. Farimah Farahmandi, University of Florida, Cyber Security Institute

Prof. Jennifer Dworak, Southern Methodist University, Texas

Phil Byrd, Micron Technology

Lee Harrison, Siemens EDA

11:15 – 12:00 Recent advancements in 3D industry Sandeep Goel, TSMC USA

12:00 - 13:00 Workshops Lunch

13:00 - 14:00 Session 3: Special EDA End-to-End Chiplet/3D IC design and test tools Chair: Tapan Chakrabarty, Renesas Electronics America

13:00 – 13:15 Cadence Design Systems

Brion Keller

13:15 – 13:30 Synopsys Inc.

Sri Ganta

13:30 – 13:45 Siemens EDA

Anshuman Chandra

13:45 – 14:00 Industry/EDA collaboration Model to support P3537/3Dblox

Sandeep Goel, TSMC USA

14:00 – 14:10 Bio Break

14:10 – 15:50 Session 4: Advancement in 3D Test

Chair: Phil Byrd, Micron Technology

14:10 – 14:35 “IEEE 1838 in Practice: Test-Access Challenges Across the 3D Stack”

Saurabh Gupta, NVIDIA

14:35 – 15:00 “Academic Research Advancements in 3D Test”

Professor Krishnendu Chakrabarty, Arizona State University

15:00 – 15:25 “Integrated 3D test Automation”

Sri Gunta, Yervant Zorian, Grigor Tshagharyan, Synopsys Inc.

15:25 – 15:50 “Expanding the IEEE std 1838-2019 for Chiplet Marketplace”

Anshuman Chandra, Siemens EDA

15:50 – 16:00pm CLOSING REMARK